CODE NO: R09221901 | R09 | SET No - 1

II B.TECH - II SEMESTER EXAMINATIONS, APRIL/MAY, 2011
COMPUTER ORGANIZATION AND ARCHITECTURE
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks

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1.a) What is the basic trade off involved in choosing the sizes of the mantissa and the exponent in a floating point number representation?
b) Find the standard single – precision binary floating point representation of the following decimal numbers
i) 13.75 ii) 256×10^6 [7+8]

2.a) Explain the data transfer between register and memory.
b) What notation is used to represent arithmetic expression in stack organization?
c) Explain shift micro operations with an example. [5+5+5]

3.a) Explain the properties of RISC architecture.
b) Explain the stack organization in a system. [7+8]

4.a) Draw and explain typical hard wind control unit.
b) Explain the execution of a complete instruction with an example. [7+8]

5.a) A block set – associative cache consists of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks, each consists of 128 words of 16 bits length. How many bits are there in main memory and in each of TAG, SET and WORD fields?
b) Explain the working of page translation mechanism. [8+7]

6.a) Explain various DMA transfer mode.
b) Explain BISYNC protocol used in serial communication. [7+8]

7.a) Draw and explain the flow chart of far stage CPU pipeline.
b) Define with respect to pipelining
i) Clock skewing ii) through put iii) Inter stage delay.[6+9]

8. Write a short note on
a) Cache Columned Protocol
b) Hyper cubs inter connection. [7+8]

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COMPUTER ORGANIZATION AND ARCHITECTURE
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks

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1.a) A particular computer system makes use of eighteen bit binary quantities as
i) Unsigned integers ii) Signed integers in two's complement representation.
Find the range of integers which can be represented in each case?

b) In an error detection and correction system, every message of length K – bits is provided with 'r' redundancy bits. Show that, for every valid code word, there are $2^r - 1$ invalid code words in the system. [8+7]

2.a) Consider the following register transfer statements for two 4 bit registers R_1 and R_2. Every time the variable T = 1, either the content of R_2 is added to the content of R_1 if x = 1, or the content of R_2 is transferred to R_1 if x = 0. Draw the block diagram for the two 4 bit registers, 4 bit adder and MUX that selects inputs to R_1. Show how the control variable x and T select the inputs of MUX and load input to register R_1
xT: $R_1 \leftarrow R_1 + R_2$
x'T: $R_1 \leftarrow R_2$

b) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. How many selection inputs are there in each MUX? What is the size of MUXs needed? And how many MUXs are there in the bus? [8+7]

3.a) Explain the design philosophy of RISC processor.

b) Explain the difference between logic shift and arithmetic shift. [7+8]

4.a) Explain the sequence of operations needed to perform
i) Storing a word in memory ii) Fetching a word from memory.

b) Give the ways to reduce number of bits in micro instructions. [8+7]

5.a) What is Cache Coherency? Why is it necessary? Explain different approaches for cache coherency.

b) Consider a two level memory hierarchy M_1 and M_2 and let C_1, C_2 be the cost per type, t_{A1} and t_{A2} be the access times and S_1 and S_2 be memory capacities for M_1 and M_2 respectively.
i) What is the effective memory access time t_A of this hierarchy?
ii) Under what conditions will the average cost of the entire memory system approach C_2. [7+8]

6.a) Explain the data transfer types in USB.

b) Explain the asynchronous data transfer using IEEE 1394 Bus. [7+8]

7.a) Explain data and resource conflicts in the instruction pipelining.

b) Write a short note on memory interleaving. [8+7]

8. Write a note on
a) Distributed shared memory architecture
b) Parallel arbitration Technique. [8+7]

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COMPUTER ORGANIZATION AND ARCHITECTURE
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks

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1.a) Explain the single line bus structure and multiple bus structure.
b) How do we determine the instruction execution speed of a processor?
c) A 36 bit floating point binary number has eight bits plus sign for the exponent and 26 bits plus sign for the mantissa. The mantissa is a normalized representation. What are the largest and smallest positive quantities that can be represented, excluding zero?
d) Convert into 16 bit binary equivalent of given octal strings
i) 145327 ii) 177777 iii) 100000 iv) 22 [15]

2.a) Show the hardware that implements the following statements. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input
$xyT_0 + T_1 + y'T_2 : AR \leftarrow AR + 1$
b) Explain the memory operation in each case given below
i) $R_2 \leftarrow M[AR]$ ii) $M[AR] \leftarrow R_3$ iii) $R_3 \leftarrow M[R_3]$ [7+8]

3.a) Comment on VLSI realization of RISC processor.
b) Explain the functioning of n – bit combinational shift circuit. [7+8]

4.a) Write a micro program for ADD SVC, R instructions.
b) What is micro programming and micro programmed control unit?
c) What is data path? [5+5+5]

5.a) Consider a processor running a program 30% of the instructions of which require a memory read or write operation if the cache hit ratio is 0.95 instructions and 0.9 for data. When ever a cache hit ratio occurs for instruction or for data only one clock is needed which the cache miss penalty is 17 clocks to read/write on the main memory. What is the time saved by using Cache, given the total number of instructions executed is 1 million.
b) Explain the virtual memory organization. [8+7]

6.a) Explain the features of USB and what are its limitations?
b) Explain how processor responds to an interrupt? [8+7]

7.a) Draw and explain a typical functional structure of SIMD array processor.
b) What is an array processor? [8+7]

8.a) Explain the structural difference between centralized and distributed stand memory architecture.
b) What is meant by bus architecture? [8+7]

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COMPUTER ORGANIZATION AND ARCHITECTURE
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3hours **Max. Marks: 75**

Answer any FIVE questions
All Questions Carry Equal Marks

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1.a) A particular computer system makes use of a non – standard floating point number representation with a 25 bit mantissa and 10 bit exponent stored in excess 511 form. The implicit extra '1' bit of the mantissa is also utilized. Find the approximate precision and range provided by this representation.

b) Define the following
i) Execution time ii) Response time
iii) MIPS rate iv) through put rate

c) Write a short note on Block parity. [5+5+5]

2.a) Represent the following conditional control statement by two register transfer statements with control functions
If (P = 1) then ($R_1 \leftarrow R_2$) else if (Q = 1) then ($R_1 \leftarrow R_3$)

b) Using 4 bit counter with parallel load and a 4 bit adder, draw a block diagram that shows how the following statements are implemented
x : $R_1 \leftarrow R_1 + R_2$
x'y : $R_1 \leftarrow R_1 + 1$ [7+8]

3.a) Describe the factors which increase computing speed in RISC machine.

b) Give a classification of instructions. [8+7]

4.a) For a single bus organization of CPU, write a micro program for instruction ADD(R_{src}) +, R_{dt}.

b) Explain the control sequence required for branch instruction. [8+7]

5.a) Comment on the performance of two level cache system.

b) Explain the replacement algorithm for cache memory. [8+7]

6. Write a short note on
a) Programmed I/O
b) Interrupt driven I/O
c) DMA controlled I/O [15]

7.a) Explain the general instruction format of the vector processor.

b) How does conditional brands instruction affect the performance of instruction pipelining? Explain with a neat timing diagram. [7+8]

8.a) Explain the inter – processor communication using message passing and shared variable.

b) Draw and explain centralized shared memory architecture. [8+7]

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